the two-part form in compliance with Rule 6.3(b) PCT. Still further, where appropriate, the new claims include reference signs in parenthesis according to Rule 6.2(b) PCT. Moreover, the new claims have been drafted to correspond with the scope of the search conducted by the ISA.

IN THE ABSTRACT

Please replace the previously amended Abstract with new page 28. This page is being substituted to correct pagination only. No changes have been made to the abstract.

REMARKS

Regarding the observations made in the Written Opinion and in the interest of advancing the prosecution of the present application, pending claims 1-47 have been canceled herein and are replaced by new claims 1-40. Support for these amendments is provided for by the drawings and specification as originally filed. No new matter has been entered.

Comments in Response to Paragraph 2

The Examiner indicated that the amendments made under Article 34 filed simultaneous with the demand introduce new matter and are therefore not admissible. While the Applicant wholly disagrees with such conclusions, in the interest of advancing the prosecution, the applicant has canceled the pending claims 1-47 filed simultaneous with the Demand, and have introduced new claims 1-40 herewith. The new claims herein include all of the features requested by the Examiner and coincide with the scope of the search that was conducted by the ISA. As such, there is no undue intermediate generalization of the subject matter of the new claims. For example, each of the claims, including independent claims 1 and 14 recite that the square feature size of the memory cell claimed is no greater than $2F^2$.

The applicant asserts that the previous claims 1-47 filed simultaneous with the demand, and now canceled herein, were a good faith attempt to advance prosecution of this application by reducing the number of claims before the Examiner. Due to the

search backlog at the ISA, the applicant was forced to make the amendments without the benefit of the Preliminary Search Report.

Comments in Response to Paragraph 3

This paragraph is rendered moot in view of the amendments herein, as described in more detail above.

Comments in Response to Paragraph 3.1

The Examiner believes that the recitation of feature size in the claims merely amounts to a statement of the underlying problem and concludes that the technical features necessary for achieving the result should be added. Features have been added to the claims in compliance herewith in the spirit of advancing this application as set out in greater detail in response to paragraph sections 4.1 and 4.2 herein.

However, The applicant respectfully disagrees with the Examiner's conclusions. The recitation of a feature size, and particularly, a square feature size of $2F^2$ represents a *structural* limitation that sets physical limitations upon the layout of a memory cell not necessary with larger square feature sizes. For example, as is well known in the art, conventional silicon processing technology for memory devices lays out wordlines and bit lines in generally orthogonal directions. The size of each cell is thus a function of the bitline pitch (distance between adjacent bitlines) and wordline pitch (distance between adjacent wordlines).

The spacing that defines each bitline pitch and wordline pitch is defined by a number of features. Each feature takes up the same width, which is a function of the photolithographic processes used to layout the memory cells. Accordingly, a recitation of a $2F^2$ square feature size represents a *structural* relationship of the components of a memory cell that requires those components, such as the source, drain and gate of a transistor structure, to occupy no more than two features in one dimension, and one feature in an orthogonal dimension.

An example can be seen from an examination of Fig. 1 of the present application. This example is intended to be merely illustrative and not limiting to the

scope of the claimed invention. As shown, a memory cell according to the present claimed invention can have a feature size of 1F in a first dimension, which is half of the digit line pitch, and a feature size of 2F in a second dimension, which is the word line pitch. See the specification as amended herein on page 10, lines 2-7. Clearly, when inspecting Fig. 1 (also seen in Figs. 2A, and 2B), one sees unit repeating cells in both the X and Y directions. Each unit is comprised of a 2-feature width -1 bitline feature (bitline stack 210 seen in Fig. 2A) and a bitline space feature (trench 205 and gates 206). The unit also has a feature size of 2F in an orthogonal direction as seen in Fig. 2B defined by 1 wordline feature, and 1 wordline space feature.

Thus the unit has a feature size of $4F^2$. However, note that two memory cells are formed per unit. That is, each bitline 210 is shared between two cells with one cell on opposite sides thereof. Further, each bitline space feature defines the select gate, which is shared between two cells, one on each side thereof. As such, the realized feature size of each memory cell is only $2F^2$. Moreover, the fact that the memory cell is confined to a $2F^2$ space structurally limits the layout of the memory cell. For example, because the memory cell of Fig. 2 has a feature size of 2F in one dimension (the wordline plus wordline space), the memory cell must necessarily include the bitline contact and gate in the space of one feature.

The Examiner notes that the technical feature necessary for achieving the result should be added. The present pending claims further recite the structural limitation that the floating gate be substantially horizontal, formed over at least a portion of the drain, and the floating gate must be sublithographic. It is well understood in the art that sublithographic means a dimension smaller than one feature size, as the feature size is determined by the photolithography process employed to construct the memory cell. Note that this limitation defines in clear structural terms, what the claimed invention is. It should further be clear to one skilled in the art, that to define a memory cell as $2F^2$ and to recite a horizontal floating gate requires that the floating gate be sublithographic where, for example as shown in Figs. 2A and 2B, 2 features are used to define the wordline and wordline space.

Comments in Response to Paragraph 3.2

The independent claims have been amended to recite both the floating gate and the select gate, thus the claims clearly recite all of the technical features that define a memory cell.

Comments in Response to Paragraph 3.3

The Examiner asserts that the terms "sublithographic", "over" and "active area" are unclear. The applicant respectfully disagrees.

The term sublithographic is well know in the art to which the invention pertains, thus the claims do not lack clarity. Sublithographic refers to the observation that the floating gate takes up space in a first dimension that is less than one feature width. The applicant clearly defines the horizontal floating gate as being a sublithographic feature. See for example, page 11, lines 5-7.

The term "over" is clearly defined in the specification on page 18, starting at line 29. Formation "over" a substrate or layer refers to formation above or in contact with a surface of the substrate (or layer)

The term "active trench" in the claims is not unclear, and is consistent with the term usage in the specification. The term is used to distinguish the STI trenches that separate adjacent memory cells along a common bitline from the trenches used to form the select gates, which are positioned on opposite sides of the bitlines.

Comments in Response to Paragraph 4

This paragraph is rendered moot in view of the amendments herein, as described in more detail above.

Comments in Response to Paragraph 4.1

Applicant notes that a number of distinctions may be drawn between the cited relevant document D1, and the present invention as defined in the new set of claims. In particular, independent claim 1 now recites the features of a substantially

horizontal floating gate formed over at least a portion of a drain, wherein the floating gate is defined by a sublithographic feature dimension and the feature size of the memory cell is not greater than $2F^2$. These recitations define specific *structural* aspects that clearly define the present claims over the art of record.

For example, with reference to D1, as best seen in Fig. 9, the minimum realizable size of the memory cell of D1 is seen generally horizontally as 1 feature defined by the N+ Drain region, 1 feature defined by the poly 1 region 12, and atleast ½ feature defined by the N+ Source region. Only ½ feature is counted because the source is apparently shared with two adjacent memory cells. Looking depthwise, we see a wordline feature and a wordline space feature. As such, the minimum realizable square size of this structure is $5F^2$. As such, given the same photolithographic feature dimensions, the present claimed invention is only 40% of the size of the cell in D1. This results in a significantly greater packing density.

Still further, reference D1 does not teach or suggest the use of a horizontal floating gate defined by a sublithographic feature dimension. Reference D1 does not suggest the use of sublithographic features at all.

Note also that the N+ region shown in D1 is highly resistive, which places a further practical limit on the utility of the memory cell taught in D1. No strapping layers or other interfaces are provided to connect the plugs to the N+ regions. This may adversely affect the possible reduction of size of the memory cell of D1. In contrast however, as claimed in claim 14, the present invention recites a TiSi layer, formed on the substrate, a TiN layer formed on the TiSi layer, and a tungsten bitline formed on the TiN layer. One skilled in the art will recognize that the layers below the tungsten bitline serve as a strap to allow a strong electrical contact despite the resistance of the N+ regions.

Another illustrative difference between the present invention and D1 is seen in claim 8. The claimed invention recites that the source is defined by an N+ region formed over a substrate. As such, several memory cells share the same source. This allows for example, the channels to be substantially vertical. Such cannot be

guaranteed with D1 (or D2-D6 for that matter). This is because in each of D1-D6, the source (or drain) is implanted into the base of the trench that formed for the select gate. As such, there will always be an X and a Y component to the channel region. If the trench is particularly shallow, or if the floating gate that separates the source from the drain is particularly wide, then the channel in D1-D6 may not be considered substantially vertical. Rather, it can become more horizontal in nature. However, the source of the claimed invention can actually align directly under the drain for each memory cell due to the use of the N+ layer.

Comments in Response to Paragraph 4.2

Applicant notes that a number of distinctions may be drawn between the cited relevant documents D2-D6, and the present invention as defined in the new set of claims. For example, the invention in references D2 and D3 are similar in many respects to that of reference D1 thus the same arguments above apply to these references. For example, in D2, the transistor includes a drain region 60 located at the base of a trench. Source region 45 is horizontally separated from the trench by the floating gates 40. Also, as pointed out in the abstract, the feature size of the invention in D2 is $6F^2$. As such, the floating gates 40 are not sublithographic as claimed.

It should be pointed out that the differences between the present claimed invention and references D1 and D2 apply as well to reference D3. In fact, as pointed out in the present specification, the prior art comprises typical flash memory cells having a square feature size between $4.5F^2$ and $8F^2$. See the specification as amended herein on page 2, lines 18-20.

The present claimed invention, as amended herein defines over references D4-D6 in other respects. For example, in each of the references D4-D6, the floating gate is substantially vertical and positioned in the same trench as the select gate. As such, references D4-D6 do not teach a substantially horizontal floating gate at all. For example, in reference D4, see the vertical floating gate 7 and vertical select gate 8. In reference D5, see vertical floating gates 325 and vertical select gates XG(N) in Figs. 3A-, 12 and 13. In reference D6, the gates are defined by vertical gate electrodes 30 and 40.

Placing the floating gate in the sidewall of the trench, as in reference D4-D6 results in the floating gate being aligned to a <1 1 1> plane or other crystallographic structures that have a higher density of bonds. Such a placement typically results in an inferior oxide resulting in retention, cycling and trapping problems within the memory cell. However, the present claimed invention provides a substantially horizontal floating gate and is arranged in the <1 0 0> plane thereby avoiding the above-mentioned problems. See the present specification as amended herein starting on page 17, lines 18-25.

In one embodiment of reference D5, a 2F2 structure is disclosed. However, to achieve that cell layout, the floating gate 325 is formed in the same trench as the select gate and is thus aligned vertically. As pointed out in the present specification, positioning the floating gate horizontally and being positioned directly over the vertical channel allows for increased efficiency in programming. See the present specification as amended herein on page 12, lines 8-10.

Comments in Response to Paragraph 5

The dependent claims as amended herein are now believed to comply with Article 33(3) PCT because each dependent claim depends from a base claim which, as amended herein, satisfies the requirements of inventive step.

Comments in Response to Paragraph 5.1

The sidewall spacers in the claims as amended herein, are at least partially removed during processing, and are used to construct the sublithographic floating gates claimed herein. As none of the references D1-D6 teach or suggest sublithographic, horizontal floating gates, the applicants believe that it would not be obvious to one skilled in the art to construct sublithographic horizontal floating gates defined by such removable spacers.

Comments in Response to Paragraph 5.2

As pointed out above, the applicant believes that the independent claims as amended herein, and from which the above claims depend, defines over the cited art D1-D6. As such, the claims are proper.

Comments in Response to Paragraph 6.1

The background has been amended herein to disclose the references D1-D6 cited herein. No new matter has been added.

Comments in Response to Paragraph 6.2

The claims have been presented herein in two-part form where appropriate in accordance with Rule 6.3(b) PCT.

Comments in Response to Paragraph 6.3

The claims have been amended to include reference signs placed in parenthesis where appropriate in accordance with Rule 6.2(b) PCT.

CONCLUSION

For all of the above-stated reasons, the amendments discussed herein are believed to distinguish the present claims over the prior art of record. Accordingly, the applicant assert that claim the claims as amended herein meet the requirements of novelty under Art. 33(2) PCT and inventive step under Art. 33(3) PCT.

Reconsideration of the pending claims is requested. Should the Examiner find the arguments herein as unpersuasive, the Examiner is encouraged to contact the undersigned or to issue an additional written opinion pursuant to Rule 66.4(a) PCT.

Respectfully submitted,

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Version With Markings To Show Changes Made to the Specification

The paragraph on page 2, starting at line 10 has been amended as follows:

Memory devices can be created using 2-dimensional structures or using 3-dimensional structures. The 2-dimensional structures are also referred to as planar structures. Generally, 3-dimensional structures yield smaller cell sizes than planar structures. SRAMs and DRAMs have been designed using 3-dimensional structures, however few flash memory cells are fabricated using 3-dimensional structures. Most flash memory cells are fabricated using planar structures. Some flash memory cells have been fabricated using 3-dimensional structures, but they are, generally, in the size range of 4.5 F^2 to 8 F^2 which are not significantly smaller than flash memory cells fabricated using planar structures. For example, U.S. Patents 4,964,080 and 5,495,441 each disclose a three dimensional memory cell including an integral select transistor. However, the size of the memory cell is no smaller than $5F^2$. Similarly, WO 99/43030 discloses a vertical MOS transistor that includes two gate electrodes. However, the overall dimensions of the transistor are $6F^2$. Relatively smaller dimensions have been realized, such as is disclosed in U.S. Patent Nos. 5,936,274 and 6,091,105 and Japanese Abstract Laid Open 03280580. However, the smaller dimensions are achieved by forming the floating gate in the sidewall of the same trench that the vertical select gate is formed in. However, this results in the floating gate formed in a <1 1 1> plane or other plane that has a higher density bond. This placement typically results in inferior oxide resulting in retention, cycling and trapping problems with the memory cell.